REMARKS

Claims 1-3, 5-9, 21-23, and 25-33 are all the claims presently pending in the application. Claims 4 and 24 have been canceled and their limitations combined with those of independent claims 1, 21, and 31.

Entry of this §1.116 Amendment is proper. Since the amendments above narrow the issues for appeal and since such features and their distinctions over the prior art of record were discussed earlier, such amendments do not raise a new issue requiring a further search and/or consideration by the Examiner. As such, entry of this Amendment is believed proper and is earnestly solicited. No new matter has been added.

It is noted that the claims have been amended solely to more particularly point out Applicant's invention for the Examiner, and not for distinguishing over the prior art, narrowing the claim in view of the prior art, or for statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached pages are captioned "**Version with markings to show changes made**".

Claims 1-3, 5-6, 9, 21-23, 25, and 27-33 stand rejected under 35 U.S.C. §102(b) as being anticipated by Sasaki et al (JP 09-145965) (hereinafter "Sasaki").

Claims 1, 6-8, and 29-30 are rejected under 35 U.S.C. §102(b) as being anticipated by Tada (U.S. Patent No. 5,684,902) (hereinafter "Tada").

Claims 7-8 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sasaki.

These rejections are respectfully traversed in view of the discussion below.

I. THE CLAIMED INVENTION

Applicant's invention, as defined for example in independent claim 1, is directed to a semiconductor laser diode chip and a method for mounting the chip onto a substrate.

A feature of the present invention includes first and second measurement marks at

positions relative to an active layer which are used to correctly position the chip with relation to the active layer and the measurement marks. The first mark is constructed by a thin line formed on an upper portion of the active layer.

With such features, it is possible to accurately position an LD chip to a substrate using a passive alignment technique even when there have been errors in a production process (e.g. see page 4, lines 9-12 and page 5, lines 1-13).

An exemplary configuration of the inventive structure is shown in Fig. 5 of the application.

The conventional structures, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such advantages.

Indeed, such features are clearly not taught or suggested by the cited references.

II. THE PRIOR ART REFERENCES

The Examiner asserts that:

> *[regarding claims 1-6, 9, 21-25, 27-33] Sasaki et al. discloses the claimed invention. Figure 1 illustrates a semiconductor laser chip comprising a first mark, a second mark...Also note figure 2 which illustrates a first pair of marks (5) and a second pair of marks (14).*
>
> *[regarding claims 1, 6-8, 29-30] Tada et al discloses the claimed invention. Figure 3a-3c illustrates a semiconductor laser chip comprising a first mark and a second mark.*

However, Applicant respectfully disagrees.

A feature of the present invention, in a non-limiting embodiment as defined, for example, by independent claim 1 (and substantially similarly by independent claims 21 and 31), and as shown for example in Fig. 5, is that the first mark (e.g., reference numeral 19; all reference numerals used herein being solely for the Examiner's understanding and convenience and not for limiting the claims in any way) is constructed by a thin line formed on an upper portion of the active layer 11. With this first mark formed on an upper portion of the active layer 11, shifting amounts of the relative position of positioning marks 15, 16 to an active layer 11 is easily accomplished. Neither Sasaki nor Tada teaches or suggests such

features.

Instead, in sharp and fundamental contrast to the present invention, Sasaki discloses that a position of a laser diode 1 is given correctly for a light arrayed waveguide grating 12 based on picture signals of markers 5 and 14 obtained by irradiation of light from above or below a board 10.

Accordingly, although a first marker 5 and a second marker 14 are described in Sasaki, neither are formed on an upper portion of a laser output portion 6. Further, Applicant notes that Fig. 1 of Sasaki discloses an electrode 4a, which is not a marker. Thus, Sasaki does not teach or suggest "*said first mark is constructed by a thin line formed on an upper portion of said active layer*", as defined by independent claim 1 (and similarly by independent claims 21 and 31).

Regarding the rejection of claims 1, 6-8, and 29-30 as being anticipated by Tada, Fig. 3(c) of Tada discloses markers 19 provided on the substrate 1 and the semiconductor laser chip 3. As shown in Fig. 3(c), however, they are not formed on the optical fiber 6. Thus, Tada also does not teach or suggest "*said first mark is constructed by a thin line formed on an upper portion of said active layer*", as defined by independent claim 1.

Thus, Applicant submits that there is no teaching or suggestion of the present invention in the disclosure of Sasaki and Tada. That is, Sasaki and Tada do not teach or suggest that the first mark is constructed by a thin line formed on an upper portion of the active layer.

Hence, turning to the clear language of independent claim 1 (and substantially similarly of independent claims 21 and 31), there is no teaching or suggestion of "*[a] semiconductor laser diode chip comprising:*

a first mark formed at a predetermined position with respect to an active layer on a face opposed to a substrate to which the chip is mounted; and

a second mark that satisfies a predetermined relative position relation to said first mark and is positioned oppositely to a substrate-side mark formed on said substrate at mounting time to said substrate,

wherein said first mark is constructed by a thin line formed on an upper portion of said active layer " (emphasis Applicant's).

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, dependent claims 2-3 and 5-9 when combined with independent claim 1, and

dependent claims 22-23 and 25-30 when combined with independent claim 21, and 32-33 when combined with independent claim 31, respectively define additional novel and non-obvious features.

Also, the other prior art of record has been reviewed, but it too even in combination with Sasaki and Tada fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-3, 5-9, 21-23, and 25-33, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 4 and 24 have been canceled without prejudice or disclaimer.

The claims have been amended as follows.

1. (Amended) A semiconductor laser diode chip comprising:

a first mark formed at a predetermined position with respect to an active layer on a face opposed to a substrate to which the chip is mounted; and

a second mark that satisfies a predetermined relative position relation to said first mark and is positioned oppositely to a substrate-side mark formed on said substrate at mounting time to said substrate,

wherein said first mark is constructed by a thin line formed on an upper portion of said active layer.

21. (Amended) A semiconductor laser diode chip with an active layer mounted on a substrate, comprising:

a first pair of marks formed in the vicinity of said active layer and straddling said active layer; and

a second pair of marks straddling said active layer, said second pair of marks located at a further distance from said active layer than said first pair of marks,

wherein said second pair of marks align with a pair of substrate side marks formed at a position opposed to said second pair of marks, and

wherein said first pair of marks comprises lines formed on an upper portion of said active layer.

31. (Amended) A semiconductor laser diode chip to be mounted on a substrate for an optical module, comprising:

an active layer;

a positioning-type mark in a vicinity of said active layer; and

a measurement-type mark located between said active layer and said positioning-type

mark,

wherein said positioning-type mark is constructed by a thin line formed on an upper portion of said active layer.